

CLAIMS

1. A data processing system comprising:
5 a memory for storing operands;
at least one general purpose register; and
processor circuitry for executing at least a first instruction and a
second instruction subsequent to the first instruction, the
first instruction transferring a stream of data elements
10 between the memory and the at least one general purpose
register and to be queued in at least one of the memory and
the at least one general purpose register, wherein the second
instruction comprises at least a first source operand, and
conditionally dequeuing a portion of the stream of data
15 elements based on the at least one general purpose register
appearing as a source operand of the second instruction.
2. The data processing system of claim 1 wherein conditionally dequeuing
the portion of the stream of data elements is performed when the at least one
20 general purpose register is used as a source operand for a predetermined type of
function specified by the second instruction.
3. The data processing system of claim 1 wherein conditionally dequeuing
the portion of the stream of data elements is performed based on a value of a
25 control field of the second instruction.

4. The data processing system of claim 1 wherein the second instruction further comprises a second source operand, and the conditional dequeuing is performed when the at least one general purpose register appears as the first source operand, and the conditional dequeuing is not performed when the at
5 least one general purpose register appears as the second source operand.

5. A method of selectively dequeuing data elements in data processing system comprising:

10 providing a memory for storing operands;
providing at least one general purpose register; and
executing at least a first instruction and a second instruction
subsequent to the first instruction;
transferring a stream of data elements between the memory and the
at least one general purpose register in response to the first
15 instruction;
queueing the stream of data elements in at least one of the memory
and the at least one general purpose register;
executing a second instruction subsequent to the first instruction,
the second instruction comprising at least a first source
20 operand; and
conditionally dequeuing a portion of the stream of data elements
based on the at least one general purpose register appearing
as the source operand of the second instruction.

25 6. The method of claim 5 further comprising conditionally dequeuing the portion of the stream of data elements when the at least one general purpose

register is used as a source operand for a predetermined type of function specified by the second instruction.

7. The method of claim 5 further comprising

5 providing a second source operand within the second instruction;
and

conditionally dequeuing the portion of the stream of data
elements when the at least one general purpose register
appears as the first source operand, and not performing
10 conditional dequeuing when the at least one general
purpose register appears as the second source operand.

8. A data processing system comprising:

a memory for storing operands;
15 at least one general purpose register; and
processor circuitry for executing a plurality of instructions, a first
one of the plurality of instructions transferring a stream of
data elements between the memory and the at least one
general purpose register and to be queued in at least one of
20 the memory and the at least one general purpose register,
and conditionally dequeuing a portion of the stream of data
elements in response to a second one of the plurality of
instructions corresponding to a predetermined instruction
within a proper subset of the plurality of instructions.

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9. The data processing system of claim 8 wherein the processor circuitry further conditionally dequeues the portion of the stream of data elements based on the at least one general purpose register appearing as a source operand of the second one of the plurality of instructions.
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10. The data processing system of claim 8 wherein the processor circuitry further conditionally dequeues the portion of the stream of data elements based on a value of a control field of the second one of the plurality of instructions.
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11. A method of selectively dequeuing data elements in a data processing system comprising:
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- providing a memory for storing operands;
- providing at least one general purpose register; and
- executing a plurality of instructions, a first one of the plurality of instructions transferring a stream of data elements between the memory and the at least one general purpose register; queueing the stream of data elements in at least one of the memory and the at least one general purpose register; and
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- conditionally dequeuing a portion of the stream of data elements in response to a second one of the plurality of instructions corresponding to a predetermined instruction within a proper subset of the plurality of instructions.
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12. The method of claim 11 further comprising further conditionally dequeuing the portion of the stream of data elements based on the at least one

general purpose register appearing as a source operand of the second one of the plurality of instructions.

13. A data processing system comprising:

5 a memory for storing operands;
 at least one general purpose register; and
 processor circuitry for executing a plurality of instructions, a first
 one of the plurality of instructions transferring a stream of
 data elements between the memory and the at least one
10 general purpose register and to be queued in at least one of
 the memory and the at least one general purpose register,
 conditionally enqueueing a portion of the stream of data
 elements based on the at least one general purpose register
 appearing as a destination operand of a second one of the
15 plurality of instructions.

14. The data processing system of claim 13 wherein enqueueing is performed
in response to the second one of the plurality of instructions corresponding to a
predetermined instruction within a proper subset of the plurality of instructions.

20 15. A method of selectively enqueueing data elements in a data processing
system comprising:

 providing a memory for storing operands;
 providing at least one general purpose register; and
25 executing a plurality of instructions, a first one of the plurality of
 instructions transferring a stream of data elements between

the memory and the at least one general purpose register and to be queued in at least one of the memory and the at least one general purpose register; and

conditionally enqueueing a portion of the stream of data elements based on the at least one general purpose register appearing as a destination operand of a second one of the plurality of instructions.

16. The method of claim 15 wherein enqueueing is performed additionally in response to the second one of the plurality of instructions corresponding to a predetermined instruction within a proper subset of the plurality of instructions.

17. A data processing system comprising:
a memory for storing operands;
at least one general purpose register; and
processor circuitry for executing at least a first instruction and a second instruction subsequent to the first instruction, the first instruction transferring a stream of data elements between the memory and the at least one general purpose register and to be queued in at least one of the memory and the at least one general purpose register, wherein the second instruction comprises at least a first destination operand, and conditionally enqueueing a portion of the stream of data elements based on at least one general purpose register appearing as a destination operand of the second instruction.

18. The data processing system of claim 17 wherein the conditional enqueueing is performed when the at least one general purpose register is used as the first destination operand for a predetermined type of function specified by the second instruction.

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19. The data processing system of claim 17 wherein the second instruction further comprises a second destination operand and the conditional enqueueing is performed when the general purpose register appears as the first destination operand and the conditional enqueueing is not performed when the general purpose register appears as the second destination operand.

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20. A data processing system comprising:

a memory for storing operands;

at least one general purpose register; and

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processor circuitry for executing at least a first instruction and a

second instruction subsequent to the first instruction, the

first instruction transferring a stream of data elements

between the memory and the at least one general purpose

register and to be queued in at least one of the memory and

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the at least one general purpose register, wherein the first

instruction further specifying a number of data elements to

be transferred, and conditionally dequeuing a plurality of

data elements from the portion of the stream of data

elements based on the at least one general purpose register

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appearing as a source operand of the second instruction.

21. The data processing system of claim 20 wherein the stream of data elements is further specified by a control field within the first instruction.

22. The data processing system of claim 20 wherein size of the stream of data elements is further specified by the instruction.

23. The data processing system of claim 22 wherein the first instruction specifies size of the stream of data elements as a field in the instruction.

24. The data processing system of claim 22 wherein the first instruction specifies size of the stream of data elements by defining a storage location that contains the size of the stream of data elements.

25. A data processing system comprising:

a memory for storing operands;

at least one general purpose register; and

processor circuitry for executing at least a first instruction and a

second instruction subsequent to the first instruction, the

first instruction transferring a stream of data elements

between the memory and the at least one general purpose

register and to be queued in at least one of the memory and

the at least one general purpose register, wherein the first

instruction further specifying the number of data elements to

be transferred, and conditionally enqueueing a plurality of

data elements from the portion of the stream of data

elements based on the at least one general purpose register
appearing as a destination operand of the second instruction.

26. The data processing system of claim 25 wherein the stream of data
5 elements is further specified by a control field within the first data processing
instruction.

27. The data processing system of claim 25 wherein a size of the plurality of
data elements is further specified by the first data processing instruction.

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28. The data processing system of claim 27 wherein the first data processing
instruction specifies size of the plurality of data elements as a field in the
instruction.

15 29. The data processing system of claim 27 wherein the first data processing
instruction specifies size by defining a storage location that contains the size of
the plurality of data elements.

30. A data processing system comprising:
20 a memory for storing operands;
at least one general purpose register; and
processor circuitry for executing a plurality of instructions, a first
one of the plurality of instructions transferring a stream of
data elements between the memory and the at least one
25 general purpose register and to be queued in at least one of
the memory and the at least one general purpose register,

and conditionally performing at least one of enqueueing and dequeueing of a portion of the stream of data elements in response to a control field within a second one of the plurality of instructions.

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31. The data processing system of claim 30 wherein the processor circuitry further conditionally performs at least one of enqueueing and dequeueing of the portion of the stream of data elements based on the at least one general purpose register appearing as an operand of the second one of the plurality of instructions.

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32. The data processing system of claim 30 wherein the processor circuitry further conditionally performing at least one of enqueueing and dequeueing the portion of the stream of data elements based on a value of a control field of the second one of the plurality of instructions.

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